



Attorney's Docket No. 904640.P019

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Yervant Zorian et al.

Examiner: Kerveros, James C.

Application No.: 10/664,190

Art Unit: 2138

Filed: September 16, 2003

For: A METHOD AND APPARATUS FOR A  
COMMAND BASED BIST FOR  
TESTING MEMORIES

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed for applications filed after June 30, 2003). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on December 6, 2006.  
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Shannon Tinsley

(Typed or printed name of person mailing correspondence)

S Tinsley

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12/6/06

(Date)

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  X   37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

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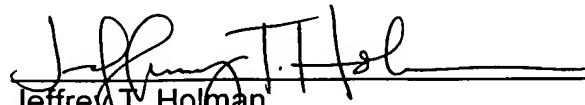
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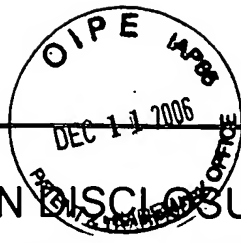
Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 12/6/06

  
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Substitute for Form 1449/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

**Complete if Known**

Application Number	10/664,190
Filing Date	September 16, 2003
First Named Inventor:	Yervant Zorian et al.
Art Unit	2138
Examiner Name	Kerveros, James C.
Attorney Docket Number	004640.P019

Sheet 1 of 2

**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (If known)				
		US-	6,237,123	05-22-2001	Ilyoung Kim et al.	
		US-	6,205,564	03-20-2001	Ilyoung Kim et al.	
		US-	6,085,334	07-04-2000	Giles	
		US-	6,317,846	11-13-2001	Higgins et al.	
		US-	5,570,374	10-29-1996	Yau et al.	
		US-	6,304,989	10-16-2001	Kraus et al.	
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		US-	6,397,349	05-28-2002	Higgins et al.	
		US-	6,067,262	05-23-2000	Irrinki et al.	
		US-	5,583,463	12-10-1996	Merritt	
		US-	5,608,678	03-04-1997	Lysinger	
		US-	6,396,760 B1	05-28-2002	Behara et al.	
		US-	6,181,614 B1	01-30-2001	Aipperspach et al.	
		US-	6,255,836 B1	07-03-2001	Scharz et al.	
		US-	6,496,946 B2	12-17-2002	Bannatyne et al.	
		US-	6,510,398 B1	01-21-2003	Kundu et al.	
		US-	6,519,202	02-11-2003	Shubat et al.	
		US-	6,574,757	03-03-2003	Park et al.	
		US-	6,654,202	11-18-2003	Phan, Tuan L.	
		US-	6,691,252	02-10-2004	Hughes et al.	
		US-	6,766,468 B2	07-20-2004	Barth et al.	
		US-	6,795,942	09-21-2004	Schwarz, William D.	
		US-	6,415,344	07-02-2002	Jones et al.	
		US-	7,149,921	12-12-2006	Zorian et al.	
		US-	10/236,248	09-05-2002	Zorian et al.	
		US-				

Examiner Signature	Date Considered
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup>For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. <sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup>Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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<b>Sheet</b>	2	<b>of</b>	2	Attorney Docket Number	004640.P019
<b>NON PATENT LITERATURE DOCUMENTS</b>					
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T <sup>2</sup>
	✓	CHANG, Tsin-Yuan and ZORIAN, Yervant: "Tutorial 2: SoC Testing and P1500 Standard," Asian Test Symposium 2000: 492			
	✓	MARINISSEN, Erik Jan, et. al.: "Wrapper Design for Embedded Core Test," ITC 2000: 911-920.			
	✓	ZORIAN, Yervant and SHOUKOURIAN, Samuel: "Embedded-Memory Test and Repair: Infrastructure IP for SoC Yield," IEEE CS and IEEE CASS May-June 2003: 58-66			
	✓	BENSO, Alfredo, et. al.: "HD2BIST: a Hierarchical Framework for BIST Scheduling, Data Patterns Delivering and Diagnosis in SoCs," ITC 2000: 892-901			
	✓	GIZOPOULOS, Dimitris, et. al.: "Low Power/Energy BIST Scheme for Datapaths," VTS 2000: 23-28			
	✓	VARDANIAN, Valery A. and ZORIAN, Yervant: "A March-based Fault Location Algorithm for Static Random Access Memories," MDTD 2002: 256-261			
	✓	BENSO, Alfredo, et. al., "HD-BIST: A Hierarchical Framework for BIST Scheduling and Diagnosis in SoCs," ITC 1999: 1038-1044			

Examiner Signature		Date Considered	
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